ABSTRACT

A delay lock loop circuit for delaying a reference clock to lock a delayed clock. The delay lock loop circuit includes a clock divider for dividing a frequency of the reference clock by N to generate a frequency-divided clock, a programmable delay circuit electrically coupled to the clock divider for delaying the frequency-divided clock to generate the delayed clock, a 180° phase detector electrically coupled to the programmable delay circuit for detecting a phase change of the delayed clock, and a delay lock loop controller electrically coupled to the programmable delay circuit and the 180° phase detector for programming the programmable delay circuit to lock the delayed clock according to the phase change.